ABSTRACT

In a method for operating a matrix-addressable ferroelectric or electret memory device a first plurality of voltage differences is applied across a first and a second set of electrodes in a matrix-addressable array when data are read from the ferroelectric memory cells thereof, and a second plurality of voltage differences is applied across the first and the second set of electrodes in the case where data are refreshed or rewritten to the ferroelectric memory cells. In each case the first and second plurality of voltage differences correspond to sets of potential levels as predefined by a voltage pulse protocol comprising time sequences of voltage pulses. At least one parameter indicative of a change in a memory cell response is determined and used for determining at least one correction factor for the voltage pulses, whereby at least one pulse parameter thereof is adjusted in accordance with the at least one correction factor.

A ferroelectric or electret memory device for implementing the above method comprises means for determining a least one parameter indicative of a change in a memory cell response, a calibration memory connected with said means for determining a correction factor for the change in a memory cell response, and control circuits for adjusting pulse parameters as applied to read and write operations in the memory device.

Figs. 7a, 8